In the Claims

In this divisional application, please cancel claims 1-13.

Please add the following new claims:

41. In an information processing system, having a plurality of modules including a processor, a cache memory, a main memory and a plurality of I/O devices, a data streamer for performing data transfer operations between said modules comprises:

a channel state memory configured to store a first allocated channel information corresponding to a data transfer operation from a source module to said data streamer, and further configured to store a second allocated channel information corresponding to said data transfer operation from said data streamer to a destination module; and

a buffer memory allocated to said data transfer operation for receiving data provided by said source module in accordance with said first allocated channel information and providing said received data to said destination module in accordance with said second allocated channel information.

42. The data streamer in accordance with claim 41 wherein said channel state memory stores information corresponding to a plurality of data transfer operations between said modules.

43. The data streamer in accordance with claim 41, wherein a buffer memory is allocated for each one of said data transfer operations and the size of said buffer memory variably changes in accordance with the size of data in a corresponding data transfer operation.

The data streamer in accordance with claim 3 wherein the data transfer rate from a source module to a corresponding buffer in said buffer memory, is different than the data transfer rate from said buffer memory to a destination module.

The data streamer in accordance with claim 4 wherein said first allocated channel information includes a first channel descriptor, wherein said data transfer operation from a source module to said buffer is accomplished in accordance with said first channel descriptor.

The data streamer in accordance with claim 5, wherein said second allocated channel information includes a second channel descriptor, wherein said data transfer operation from said buffer to said destination module is accomplished in accordance with said second channel descriptor.

The data streamer in accordance with claim 6, wherein said first and said second channel descriptors have a different format.

The data streamer in accordance with claim 1 wherein said data transfer operation from a source module to a destination module includes a data cache operation having a coherent allocation policy.

The data streamer in accordance with claim 1 wherein said data transfer operation from a source module to a destination module includes a data cache operation having a

coherent no-allocation policy.

10. The data streamer in accordance with claim 1 wherein said data transfer operation from a source module to a destination module includes a data cache operation having a non-coherent no-allocation policy.

11. In an information processing system, having a plurality of modules including a processor, a cache memory, a main memory and a plurality of I/O devices, a data streamer for performing data transfer operations between said modules comprises:

a channel state memory configured to store a plurality of allocated channel information defining a plurality of source channels each of which corresponding to a data transfer operation from a source module to said data streamer, and further configured to store a plurality of allocated channel information defining a plurality of destination channels each of which corresponding to said data transfer operation from said data streamer to a destination module;

a buffer memory allocated to said data transfer operation for receiving data provided by said source module in accordance with said first allocated channel information and providing said received data to said destination module in accordance with said second allocated channel information;

a transfer engine coupled to said channel state memory and configured to service a plurality of data paths, on a preassigned priority order, wherein each data path is defined by at least one channel having corresponding information stored in said channel state memory, said data path also defined by said buffer memory corresponding to said channel

12. The data streamer in accordance with claim 11, wherein a predetermined buffer space within said buffer memory is allocated for each one of said data transfer operations and the size of said buffer space variably changes in accordance with the size of data in a corresponding data transfer operation.

13. The data streamer in accordance with claim 12 wherein the data transfer rate from a source module to a corresponding buffer space in said buffer memory, is different than the data transfer rate from said buffer space to a destination module.

14. The data streamer in accordance with claim 13 wherein each of said source channels includes a first channel descriptor, wherein said data transfer operation from a source module to said buffer is accomplished in accordance with said first channel descriptor.

15. The data streamer in accordance with claim 13, wherein said destination channel includes a second channel descriptor, wherein said data transfer operation from said buffer space to said destination module is accomplished in accordance with said second channel descriptor.

16. The data streamer in accordance with claim 15, wherein said first and said second channel descriptors have a different format.

17. The data streamer in accordance with claim 16 wherein said data transfer

operation from a source module to a destination module includes a data cache operation having a coherent allocation policy.

18. The data streamer in accordance with claim 16 wherein said data transfer operation from a source module to a destination module includes a data cache operation having a coherent no-allocation policy.

19. The data streamer in accordance with claim 16 wherein said data transfer operation from a source module to a destination module includes a data cache operation having a non-coherent no-allocation policy.

20. In an information processing system, having a plurality of modules including a processor, a cache memory, a main memory and a plurality of I/O devices, a method for performing data transfer operations between said modules comprising the steps of:

storing a first allocated channel information corresponding to a data transfer operation from a source module to a buffer memory;

storing a second allocated channel information corresponding to said data transfer operation from said buffer memory to a destination module;

receiving data provided by said source module in accordance with said first allocated channel information; and

providing said received data to said destination module in accordance with said second allocated channel information.

21. The method in accordance with claim 20 further comprising the step of storing a plurality of said channel information each of which corresponding to a data transfer operation.

22. The method in accordance with claim 21, further comprising the step of allocating a buffer memory space within said buffer memory , and changing the size of said buffer memory space in accordance with the size of data in a corresponding data transfer operation.

23. The method in accordance with claim 22 further comprising the step of setting the data transfer rate from a source module to a corresponding buffer memory space at a different rate than the data transfer rate from said buffer memory space to a destination module.

24. The method in accordance with claim 23, further comprising the step of transferring data in accordance with a predetermined channel descriptor.

25. The method in accordance with claim 24 data streamer in accordance with claim 14 wherein said data transfer operation from a source module to a destination module includes a data cache operation having a coherent allocation policy.

26. The data streamer in accordance with claim 20 further comprising the step of

providing data transfers having a data cache operation with a coherent no-allocation policy.

The data streamer in accordance with claim 20 further comprising the step of providing data transfers having a data cache operation with a non-coherent no-allocation policy.--

Remarks

In the parent application, the Examiner subjected claims 1-40 to a restriction or election requirement. Applicant selected to prosecute claims 1-13 in the parent application, and canceled claims 14-40 in that application without prejudice. Claims 1-27 of this divisional application correspond to claims 14-40 that were canceled in the parent application. Applicant hereby requests that new claims 1-27 be considered in this divisional application. An early and favorable action on the merits is respectfully requested.

Respectfully submitted,

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